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In the Specification:

Please substitute the following paragraphs for the corresponding paragraphs beginning at the indicated location in the specification as originally filed.

(Para 0007)

Another complication with the placement of gates ~~of~~ on opposite sides of the channel is that many known fabrication processes provide a gate structure which wraps around the conduction channel in a single body. Therefore the entire gate can only be driven to a single voltage even though it is desirable in some circumstances to place different voltages on opposite sides of the conduction channel. Conversely, true dual-gate transistor designs that have separated gate electrodes generally ~~precent~~ present severe difficulties in forming connections to the separated gate electrodes.

(Para 0021)

The SOI wafer, as described above will generally include a thick so-called handling wafer or substrate 10 covered by a buried oxide (BOX) 12. Monocrystalline semiconductor layer 14, in turn, covers the buried oxide 12. Doping levels are relatively low in the preferred embodiment of this device, with the requirement that the channel be fully depleted. Typical doping levels are preferably in the ~~1015~~ 10^{15}/cm^3 to ~~1017~~ 10^{17}/cm^3 range with the high ~~1016~~ 10^{16}/cm^3 range being preferred. The process of the present invention begins by forming a layer of pad nitride of about 100 nm thickness and a pad oxide of about 3 - 10 nm thickness over the silicon and patterning the nitride using a patterned resist 18. The silicon height will determine device width and is preferably in the range of 50-200 nm. Many suitable resists and lithographic techniques for patterning them

are familiar to those skilled in the art and specifics thereof are unimportant to the practice of the invention.

(Para 0023)

Then, as shown in Figure 2, the narrow conduction channels are formed by further etching the silicon to undercut the nitride with a wet etch (e.g. NH4OH based) or a chemical downstream isotropic etch (CDE) which is selective between the silicon and the BOX to achieve the desired channel width. The channel height is preferably determined by the full thickness of monocrystalline layer 16. The gate dielectric is then grown or deposited to an oxide equivalent thickness of 1 - 5 nm, with a thickness of 1 - 2 nm being preferred. Silicon dioxide, silicon nitride or higher-k could all be used. The gate material 20 is then deposited, polished and recessed below the nitride surface, as shown. Note that polysilicon is illustrated and may be preferred because of the ease of processing but alternate layers including SiGe alloys of metal layers could be used. In the polishing process, the nitride serves as a polish stop and the gate material is recessed using an isotropic etch. The polysilicon is recessed with a preferably anisotropic etch selective to the pad nitride.

(Para 0025)

Referring now to Figure 3, in the first alternative embodiment of the invention a disposable hard mask 41 of, for example borosilicate glass (BSG), arsenic doped glass (ASG), other doped glass or ozone TEOS is deposited and the active area patterned as shown in Figure 3A using and active area mask and etch procedure to separate transistors. The active area is generally rectangular with the etched silicon forming an "H" or "I" shaped pattern within it. The ends form

the source and drain 42 of the transistor and the central regions of each are joined by a silicon conduction channel 14. The polysilicon outside the active area is etched down to the BOX 14. This etching process also removes pad nitride and monocrystalline silicon if not masked, leaving a single transistor structure, as shown, for each active area mask. However, as alluded to above, with appropriate spacing of pad nitride deposits a transistor can be formed under each pad nitride deposit. The active area masks would thus only allow separating of the gate polysilicon 20 between transistors. Even this separation of transistors may be eliminated in some applications in arrays where the gates form bit lines or word lines.

(Para 0026)

Then, silicide (preferably tungsten silicide, WsiX) is deposited preferably by chemical vapor deposition (CVD) and etched to form sidewall spacers 30 in a self aligned manner familiar to those skilled in the art. It may be necessary to deposit a thin polysilicon film prior to silicide deposition to improve the adhesion of the WSiX to the underlying silicon. It may be preferred to deposit a thin polysilicon film or other barrier film prior to silicide deposition to avoid attacking the thin silicon regions. Note that if such a barrier such as ~~Tin~~ TiN or WN is used, WSiX may be replaced by a metal such as tungsten.

(Para 0027)

Alternatively, as illustrated in Figure 3B, the disposable active area hard mask is applied and patterned and etching to the BOX 14 is performed as before. Then the hard mask is stripped and a conformal layer of polysilicon and silicide (e.g. WSiX or

silicides of cobalt or titanium) is deposited, again by chemical vapor deposition. (In addition, the silicides may be replaced by a combination of tungsten and barrier tungsten nitride, tantalum nitride, tantalum silicon nitride or any other known, low-resistance material. Additional mask material such as boron or ~~Arsenic~~ arsenic doped glass (BSG or ASG) or Ozone TEOS is applied and etched to form sidewalls 32. The silicide (and underlying polysilicon is then etched to the buried oxide and all remaining mask material is stripped. This process thus provides the preferred liner shape 34 of the silicide.

(Para 0029)

As shown in Figure 5, the transistor is substantially completed (but for upper level metallization) by standard shallow trench isolation (STI) processing in which the trenches which now exist between transistors are filled with a dielectric 49 such as oxide or nitride or a combination thereof. The STI material can then be planarized preparatory to contact formation.

(Para 0030)

Connections may then be made, as desired, to the source, drain and gate regions, preferably at locations of remaining silicide by lithographically defining and etching openings in the STI material at appropriate locations and depositing metal in the openings and on the surface as shown at 50 of Figure 5. Alternatively, a damascene gate connection 50' may be used to contact the gate polysilicon (of either gate electrode or both gate electrodes may be connected together by removing the silicon nitride and replacing it with a conductor) or contacts may be landed in the STI structure to contact the WSiX liner (Figure 3B) to make a connection to the gate liner shape as can be appreciated from the

illustration of connection 50 in Figure 5. Damascene and conventional contacts may be used in any combination. The structure also permits different potentials to be applied to either of the dual gates.